

# GI/ITG Dynamic Reconfigurable Workshop – DRS 2005

March 17<sup>th</sup> 2005, Innsbruck, Austria

## Opening Keynote

8<sup>00</sup> – 8<sup>45</sup> Peter Alfke, Xilinx Inc., USA  
*FPGA-based Crossbar Switch Uses Partial Reconfiguration*

## Session 1: Data Processing, Chair: Christian Hochberger, TU Dresden, Germany

8<sup>45</sup> – 9<sup>10</sup> Katsuaki Deguchi, Keio University, Japan  
Shohei Abe, Keio University  
Kenichiro Anjo, NEC electronics  
Toru Awashima, NEC electronics  
Hideharu Amano, Keio University  
*Implementing core tasks of JPEG2000 Encoder on Dynamically Reconfigurable Processor*

9<sup>10</sup> – 9<sup>35</sup> Faisal Suleman, Fraunhofer Institute for Communication Systems (ESK), Germany  
Dirk Eilers, Fraunhofer Institute for Communication Systems (ESK)  
Helmut Steckenbiller, Fraunhofer Institute for Communication Systems (ESK)  
Andreas Herkersdorf, Institute for Integrated Systems/TUM  
*Adaptable DSP Functions for Dynamically Reconfigurable Communication Systems*

9<sup>35</sup> – 10<sup>00</sup> Takeaki Sugimura, Tohoku University, Japan  
Yuta Konishi, Tohoku University  
Yoshihiro Nakatani, Tohoku University  
Takafumi Fukushima, Tohoku University  
Hiroyuki Kurino, Tohoku University  
Mitsumasa Koyanagi, Tohoku University  
*Dynamical Multi-Context Reconfiguration Scheme for Reconfigurable Parallel Image Processing system with Three Dimensional Structure*

10<sup>00</sup> –  
10<sup>30</sup> Coffee Break

## Session 2: Hardware/ Software Reconfigurable Systems, Chair: Peter Alfke, Xilinx, USA

10<sup>30</sup> –  
10<sup>55</sup> Jens Braunes, TU Dresden, Institut für Technische Informatik; Germany  
Steffen Köhler, TU Dresden, Institut für Technische Informatik  
Annett Königsmann, TU Dresden, Institut für Technische Informatik  
Rainer G. Spallek, TU Dresden, Institut für Technische Informatik  
*Ein Zwischenformat-Profiler für das RECAST-Framework*

10<sup>55</sup> –  
11<sup>20</sup> Michael Hübner, ITIV, University Karlsruhe, Germany  
Katarina Paulsson, ITIV, University Karlsruhe  
Marcus Stitz, ITIV, University Karlsruhe  
Jürgen Becker, ITIV, University Karlsruhe  
*Novel and Seamless Design-Flow for Partial and Dynamic Reconfigurable Systems with Customized Communication Structures based on Xilinx Virtex-II FPGAs*

11<sup>20</sup> –  
11<sup>45</sup> Heiko Hinkelmann, Technische Universität Darmstadt, Germany  
Thilo Pionteck, Technische Universität Darmstadt  
Oliver Kleine, Technische Universität Darmstadt  
Manfred Glesner, Technische Universität Darmstadt  
*Prozessorintegration und Speicheranbindung dynamisch rekonfigurierbarer Funktionseinheiten*

11<sup>45</sup> –  
12<sup>10</sup> Mohamed Taher, The George Washington University, USA  
Esam El-Araby, The George Washington University  
Tarek El-Ghazawi, The George Washington University  
*Configuration Caching in Adaptive Computing Systems Using Association Rule Mining (ARM)*

12 <sup>10</sup> - 13 <sup>30</sup>	Lunch Break
<b>Session 3:</b>	<b>Design and Methodologies, Chair: Jürgen Becker, Universität Karlsruhe (TH)</b>
13 <sup>30</sup> - 13 <sup>55</sup>	<p>Christophe Bobda, University of Erlangen-Nuremberg, Germany</p> <p>Ali Ahmadiania, University of Erlangen-Nuremberg</p> <p>Mateusz Majer, University of Erlangen-Nuremberg</p> <p>Adronis Niyonkuru, University of the Federal Armed Forces Hamburg</p> <p><i>Partial Configuration Design and Implementation Challenges on Xilinx Virtex FPGAs</i></p>
13 <sup>55</sup> - 14 <sup>20</sup>	<p>Florian Dittmann, University Paderborn, Germany</p> <p>Achim Rettberg, University Paderborn</p> <p>Fabian Schulte, University Paderborn</p> <p><i>A Y-Chart Based Tool for Reconfigurable System Design</i></p>
14 <sup>20</sup> - 14 <sup>45</sup>	<p>Mohamed Taher, The George Washington University, USA</p> <p>Tarek El-Ghazawi, The George Washington University</p> <p><i>Fast Online Placement in FPGAs</i></p>
14 <sup>45</sup> - 15 <sup>10</sup>	<p>Andres Upegui, EPFL, Switzerland</p> <p>Rico Moeckel, EPFL</p> <p>Elmar Dittrich, EPFL</p> <p>Auke Ijspeert, EPFL</p> <p>Eduardo Sanchez, EPFL:</p> <p><i>An FPGA Dynamically Reconfigurable Framework for Modular Robotics</i></p>
15 <sup>10</sup> - 15 <sup>20</sup>	<b>Closing Session</b>